IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/120,169, filed April 10, 2002, ~~pending.~~ now U.S. Patent 6,787,932, issued September 7, 2004.

Please amend paragraph number **[0040]** as follows:

[0040] Terminals 26 of circuit board 10 may be fabricated by any suitable, known technique. By way of example only, an electrolytic process that employs known dry film techniques and copper filling or plating may be used to form terminals 26. Also, each terminal 26 may be plated with a material, such as gold or another so-called "noble ~~metal",~~ metal," nickel, or a combination of different plating layers, that may enhance the adhesion and electrical connection characteristics of an intermediate conductive element thereto. Such plating may also be effected by known processes, such as by electrolytic, electroless, or immersion plating techniques.

Please amend paragraph number **[0041]** as follows:

[0041] If circuit board 10 also includes one or more recessed areas 24, each recessed area 24 may be sized and configured to receive at least some of the excess adhesive material that is forced outwardly from a die-attach location 20 of circuit board 10 as a semiconductor device is secured in position thereover. Each recessed area 24 may substantially laterally surround its corresponding die-attach location 20, as depicted in FIGs. 1 and 2. Alternatively, as shown in FIG. 4, one or more discrete recessed areas 24′ may be positioned laterally around only portions of a corresponding die-attach location 20. Further, each recessed area 24, 24′ may extend into its corresponding die-attach location 20 so as to overlap periphery 22 and to extend at least partially beneath a semiconductor device when the semiconductor device is secured into position over that die-attach location 20 (*see* FIG. 10). Recessed areas 24, 24′ may also laterally extend substantially to a periphery of each terminal 26 that corresponds to the corresponding ~~die-~~

~~attach-~~ die-attach location 20, thereby effectively increasing the height of each such terminal 26 for purposes of preventing excess adhesive material from flowing onto and contaminating connection surface 27 thereof.

Please amend paragraph number **[0055]** as follows:

[0055] Solder mask 30″, which substantially covers surface 14″, includes a single device-securing region 40″ that is aligned with and positioned over at least a portion of ~~die-attach-~~ die-attach location 20″ of circuit board 10″. In addition, dams 46″ of solder mask 30″ are aligned with and positioned laterally around corresponding terminals 26″ of circuit board 10″. As shown, dams 46″ may substantially laterally surround terminals 26″, with only connection surface 27″ of each terminal 26″ or a portion thereof being exposed through each dam 46″. A recessed area 44″ is positioned between each peripheral edge 43″ of device-securing region 40″ and dams 46″ that are located adjacent to that peripheral edge 43″. Thus, each recessed area 44″ is positioned over circuit board 10″ so as to extend laterally from a die-attach location 20″ thereof to terminals 26″ that correspond to that die-attach location 20″.